



Original Article

Combined Power Ratio Calculation, Hadamard Transform and LMS-Based Calibration of Channel Mismatches in Time-Interleaved ADCs

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Abstract: This paper presents a method for all-digital background calibration of multiple channel mismatches including offset, gain and timing mismatches in time-interleaved analog-to-digital converters (TIADCs). The average technique is used to remove offset mismatch at each channel. The gain mismatch is calibrated by calculating the power ratio of the sub-ADC over the reference ADC. The timing skew mismatch is calibrated by using Hadamard transform for error correction and LMS for timing mismatch estimation. The performance improvement of TIADCs employing these techniques is demonstrated through numerical simulations. Besides, achievement results on the field-programmable gate array (FPGA) hardware have demonstrated the effectiveness of the proposed techniques.

Keywords: Time-interleaved analog-to-digital converter (TIADC), channel mismatches, all-digital background calibration.

1. Introduction

Recently, time-interleaved analog-to-digital converters (TIADCs) are known and widely used in high-speed wireless applications [1]. It uses M sub-ADCs that have a low sampling frequency to sample the analog input signal in a time-interleaving manner. The digital output of sub-ADCs is then multiplexed together to form the digital output of TIADC. Therefore, the speed of TIADC increases M times compared to

sub-ADC, where M is the number of sub-ADCs used for time-interleaving [2-4]. However, the performance of TIADCs is severely degraded by mismatches between sub-ADCs, including offset, gain, timing, and bandwidth mismatches [4, 5]. Therefore, correcting these mismatches is a very essential requirement.

There have been several works on compensating mismatches in TIADCs [6-17]. Among these works, some researchers calibrate in either all-analog domain [6] or mixed-signal domain [7]. All-analog calibration techniques can be performed with any input signal, but analog estimation is difficult to implement and is not suitable for CMOS technology. Mixed-

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signal calibration techniques require low power consumption and small chip area. However, its correction is inaccurate and requires an additional analog circuit. Therefore, it reduces the resolution of TIADC and increases the calibration time. Moreover, they are not portable between CMOS technology nodes. Thanks to the sinking of CMOS technology, the all-digital calibration techniques are currently preferred. These techniques usually only focus on correcting one or two types of deviations (usually gain and/or timing mismatch) but do not include offset one [8-10, 12-17]. The authors in [8] are only calibrated timing mismatch by using the polyphase structure for good results. However, this technique cannot solve the offset and gain mismatches. The gain and timing mismatches have been calibrated in [12]. Nevertheless, convergence time is long and unverified on hardware. The authors in [11] corrected all three errors including offset, gain and timing mismatches. However, the main limitation of this technique is that there is an overlap between the desired signal and spurious signals when the input signal is a single tone spaced at $k\pi/M$. In our recent work [18], a calibration technique was proposed for all offset, gain, and timing mismatches with preliminary results without hardware validation.

To overcome the limitations of current techniques, this paper proposes a fully digital blind calibration technique for offset, gain and timing mismatches in TIADC. The proposed technique first calibrates the offset error by taking the average of sub-ADC output samples, and then calibrate gain by calculating the power ratio of the sub-ADC with the reference ADC. Finally, timing skew is calibrated by using Hadamard transform for correction and LMS algorithm for estimation. The effectiveness of the proposed technique is demonstrated by simulation and verification results on FPGA hardware.

The proposed technique achieves higher performance and a faster convergence speed compared with the previous techniques. This technique significantly reduces the required

hardware resources, specifically for the derivative and fractional delay filters for which no look-up table is required. In addition, the proposed technique requires only one FIR filters with fixed coefficients, thus reducing complexity and hardware resources, as compared to the bank adaptive filter techniques.

The rest of this paper is organized as follows. Section 2 introduces the TIADC model with offset, gain, and timing mismatches. Section 3 presents the proposed technique of fully digital background calibration for channel mismatches. Simulation and experimental results on FPGA hardware are analyzed and discussed in Section 4. Finally, conclusion is carried out in Section 5.

2. System Model

Consider the M -channel TIADC model consisting of offset, gain, and timing mismatches in Fig. 1. The channel mismatch of the i^{th} sub-ADC is characterized by the offset errors o_i , the gain errors g_i , and the relative timing deviations t_i for $i=0,1,\dots,M-1$. Without considering the quantization effects, the i^{th} channel's digital output can be expressed as:

$$y_i[k] = g_i x((kM+i)T - t_i) + o_i \quad (1)$$

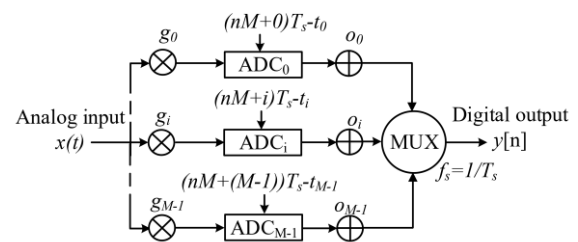


Figure 1. Model of a M -channel TIADC with offset, gain and timing mismatches.

By assuming a bandlimited input signal $X(j\Omega) = 0$, with $|\Omega| \geq B$ and $B \leq \frac{\pi}{T_s}$, the output of M -channel TIADC including the

errors: offset, gain, and timing mismatches errors is expressed as [5]:

$$\begin{aligned}
 Y(e^{j\omega}) = & \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} g_i e^{-j\left(\omega - k \frac{\omega_s}{M}\right)t_i} \cdot e^{jki \frac{2\pi}{M}} \right] \\
 & \times \left(j \left(\omega - k \frac{\omega_s}{M} \right) \right) \\
 & + \frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{jki \frac{2\pi}{M}} \delta \left(\omega - k \frac{\omega_s}{M} \right).
 \end{aligned} \tag{2}$$

This expression shows that, in the presence of all the errors, the input signal is modulated by the expression between brackets which combines gain and timing mismatch errors.

These errors appear at each $\omega_{in} \pm k \frac{\omega_s}{M}$ frequency, where ω_{in} is the input frequency. Additionally, the offset mismatch tones intervene as signal independent spurious tones at each $k \frac{\omega_s}{M}$.

3. Proposed Method

The proposed technique performs offset mismatch correction before gain and timing mismatches correction.

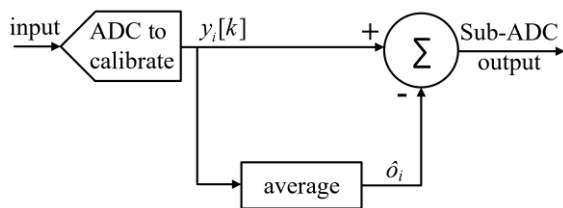


Figure 2. Offset mismatch calibration for each sub-ADC.

3.1. Offset Calibration

The offset calibration scheme is illustrated in Fig. 2. Assume that \hat{o}_i is the estimated offset mismatch value of the i^{th} channel ADC. Assume

that the input signal is Wide-Sense-Stationary (WSS), expected value of the input is approximately zero, i.e.

$$\frac{1}{N} \sum_{k=0}^{N-1} g_i x((kM + i)T_s - t_i) \approx 0.$$

Thus, estimated offset values are expressed as follows:

$$\begin{aligned}
 \hat{o}_i &= \frac{1}{N} \sum_{k=0}^{N-1} y_i[k] \\
 &= \frac{1}{N} \sum_{k=0}^{N-1} (g_i x((kM + i)T_s - t_i) + o_i) \\
 &= \frac{1}{N} \sum_{k=0}^{N-1} \underbrace{g_i x((kM + i)T_s - t_i)}_{\approx 0} + o_i \approx o_i.
 \end{aligned} \tag{3}$$

The offset error can be calibrated by firstly averaging the output of each sub-ADC over N samples as in (3) and then subtracting the average value from the ADC output as follow:

$$\begin{aligned}
 \hat{y}_{\text{offset}}[k] &= g_i x((kM + i)T - t_i) + o_i - \hat{o}_i \\
 &= g_i x((kM + i)T - t_i).
 \end{aligned} \tag{4}$$

3.2. Gain Calibration

The signal after calibration of offset mismatch is expressed in (4). The goal of gain mismatch estimation is to determine the relative gain of each sub-ADC with respect to a reference ADC, i.e. $\frac{g_i}{g_0}$. Let us assume that the

first channel is the reference channel. The authors in [19] obtained the relative gain each sub-ADC by calculating the ratio between the sum of samples' absolute values of ADC to be corrected and the reference ADC. Although this technique is easy for implementation, the performance is not high, especially the spurious-free dynamic range (SFDR). Assuming the power of the channels is the same. Inspired by the calibration method in [19], in this paper, we propose another method to calculate the relative gain. It is obtained by calculating the average power of the i^{th} ADC and the average power of a reference sub-ADC as:

$$\frac{\frac{1}{N} \sum_{k=0}^{N-1} y_0^2[k]}{\frac{1}{N} \sum_{k=0}^{N-1} y_i^2[k]} = \frac{g_0^2 P_{x(t)}}{g_i^2 P_{x(t)}} = \frac{g_0^2}{g_i^2}. \quad (5)$$

This ratio is then taken the square root and multiplied by the i^{th} sub-ADC output to produce the corrected sub-ADC output. This output have the same gain mismatch of the reference sub-ADC as shown in Fig. 3. Therefore, the gain mismatch among sub-ADC channels is the same.

Since gain calibration requires adders and multipliers running at the sampling rate of sub-ADCs, it is efficient for the hardware implementation in terms of power consumption and area.

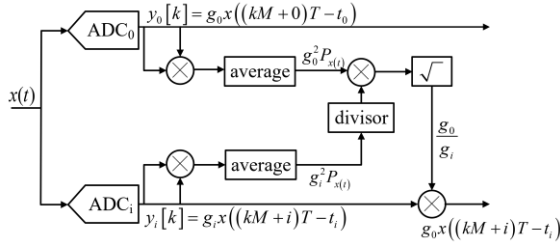


Figure 3. Gain mismatch calibration for each sub-ADC.

3.3. Timing calibration

3.3.1. Timing mismatch correction

After calibration of offset and gain mismatch, the ADC output is only timing mismatch. Thus, the ADC output can be expressed as:

$$y_i[k] = x((kM+i)T-t_i). \quad (6)$$

The timing mismatch correction technique is illustrated in Fig. 4. Assume that the sum of the timing mismatch in each channel is equal to zero $t_0 + t_1 + \dots + t_{M-1} = 0$. The overall output spectrum of the TIADC including only timing mismatch is expressed as [5]:

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} e^{-j\left(\omega - k\frac{\omega_s}{M}\right)t_i} \cdot e^{jki\frac{2\pi}{M}} \right] \times X\left(j\left(\omega - k\frac{\omega_s}{M}\right)\right). \quad (7)$$

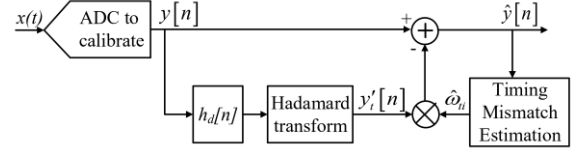


Figure 4. The calibration diagram for the timing mismatch in TIADC.

Without loss of generality, we consider the M -channel model without a quantization noise. $F_k(j\omega)$, $k = 0, 1, \dots, M-1$ are channel responses, where $-\pi < \omega \leq \pi$. Since $F_k(j\omega)$ have only timing mismatch, these channel responses are expressed as:

$$F_k(j\omega) = e^{j\omega(k-t_i)}. \quad (8)$$

To calibrate timing mismatch, we use Hadamard transform multiplied by the output signal of the ADC. This signal is called an error signal ($y_t'[n]$) which is used to removing timing skew.

$$y_t'[n] = y[n] \mathbf{H}[n] * h_d[n], \quad (9)$$

where $\mathbf{H}[n]$ is the Hadamard matrix of order M , $h_d[n]$ is the impulse response of the derivative filter.

$$h_d[n] = \begin{cases} \frac{\cos(n\pi)}{n} & (n \neq 0) \\ 0 & (n = 0) \end{cases}. \quad (10)$$

The calibrated signal $\hat{y}[n]$ is calculated by subtracting the error signal from the TIADC output $y[n]$ [20]:

$$\hat{y}[n] = y[n] - t_i' y_t'[n]. \quad (11)$$

The filter coefficients in (10) are determined by multiplying the exact coefficients with the Hanning window function. The coefficients t_i' are calculated based on the sign of the Hadamard matrix as follows:

$$\begin{bmatrix} t_0' \\ t_1' \\ \vdots \\ t_{M-1}' \end{bmatrix} \approx \frac{1}{M} \mathbf{H} \begin{bmatrix} t_0 \\ t_1 \\ \vdots \\ t_{M-1} \end{bmatrix}. \quad (12)$$

where t_i ($i = 0, 1, \dots, M - 1$) is much less than 1 and $t'_0 = 0$.

3.3.2. Timing mismatch estimation

In this section, we present the structure of the timing mismatch estimation block as shown in Fig. 5. The timing mismatch estimation block gives timing mismatch coefficients \hat{t}_i by using the LMS algorithm. These estimated values are used to create the estimated error signal $\hat{y}'_i[n]$. This signal is then subtracted from $y[n]$ to obtain the restored signal $\hat{y}[n]$ as:

$$\hat{y}[n] = y[n] - \hat{y}'_i[n], \quad (13)$$

where

$$\hat{y}'_i[\mathbf{n}] = \hat{\mathbf{t}}_i \bar{\mathbf{y}}'_i[\mathbf{n}], \quad (14)$$

with $\bar{\mathbf{y}}'_i[\mathbf{n}]$ are generated by the FIR filter $f[n]$ and Hadamard transform $\mathbf{H}[\mathbf{n}]$ as in (15). This technique requires only one FIR filter for M -channel estimation. Thus, the circuit area is reduced.

$$\bar{\mathbf{y}}'_i[\mathbf{n}] = y[\mathbf{n}] \mathbf{H}[\mathbf{n}] * h_d[n] * f[n]. \quad (15)$$

Timing mismatch coefficients \hat{t}_i can be calculated from an updating of the correlation by the LMS algorithm as follows:

$$\hat{\mathbf{t}}_i[\mathbf{n}] = \hat{\mathbf{t}}_i[\mathbf{n} - 1] + \mu \bar{\mathbf{y}}'_i[\mathbf{n}] \varepsilon[\mathbf{n}], \quad (16)$$

where μ is the step-size parameter for LMS algorithm, whereas $\varepsilon[n]$ are delayed versions of $y[n]$ after the high-pass filter $f[n]$.

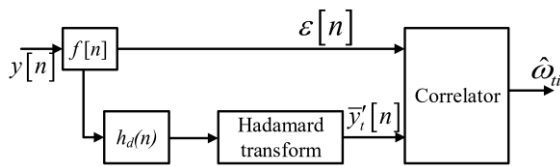


Figure 5. The timing mismatch estimation block.

4. Experimental Results

4.1. Simulation Results

MATLAB software was used for simulation to demonstrate the efficiency of the proposed technique. A 33-tap correction FIR filter, 12-bit

ADC quantization, and a sampling frequency of 2.7GHz are used. The correction FIR filter is designed with the Hanning window for truncation and delay. The simulated results of a four-channel TIADC are shown, assuming that the channel 0 without timing mismatch is the reference channel for timing mismatch calibration, as demonstrated in Table 1. The input signal is bandlimited with a variance $\sigma = 1$ and 2^{18} sample, LMS algorithm with adaptive step $\mu = 2^{-14}$. The signal-to-noise ratio (SNR) is calculated according to equation (17), (18) for $y[n]$ and $\hat{y}[n]$ as [13]:

$$SNR_y = 10 \log_{10} \left(\frac{\sum_{n=0}^{N-1} |x[n]|^2}{\sum_{n=0}^{N-1} |x[n] - y[n]|^2} \right), \quad (17)$$

$$SNR_{\hat{y}} = 10 \log_{10} \left(\frac{\sum_{n=0}^{N-1} |x[n]|^2}{\sum_{n=0}^{N-1} |x[n] - \hat{y}[n]|^2} \right). \quad (18)$$

The simulation results in Fig. 6 show the output spectrum before and after channel mismatches calibration for single-tone sinusoidal input signal which is created at $f_{in} = 0.45 f_s$. The proposed technique has completely eliminated all channel mismatches. The signal-to-noise-and-distortion ratio (SNDR) after calibration is 67.2 dB which leads to an improvement of 48.10 dB compared with the uncompensated output. Moreover, SFDR after calibration is 97.89 dB equivalent to an improvement of 77.98 dB compared with the uncompensated output. Thus, the performance of TIADC is significantly improved. Comparing

Table 1. The table of channel mismatch values

Sub ADC	Channel mismatches		
	o_i	g_i	t_i
ADC_0	0.026883	0.0365	0
ADC_1	0.091694	-0.00481	-0.00092685 T_s
ADC_2	-0.01129	-0.0047	-0.00092685 T_s
ADC_3	0.043109	-0.00782	0.00092685 T_s

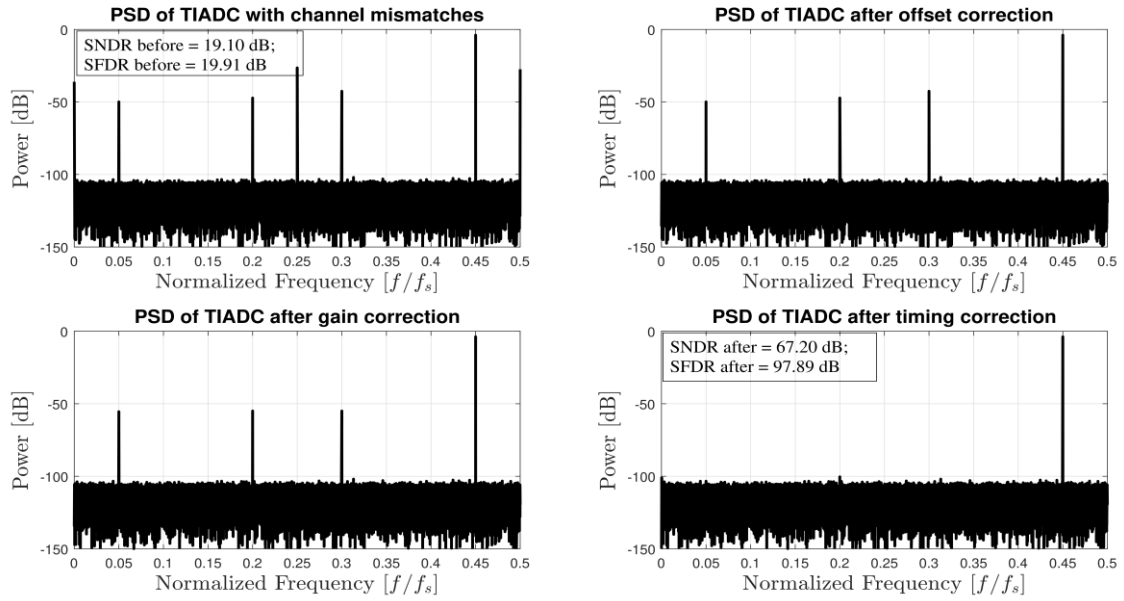


Figure 6. Output spectrum of four-channel TIADC before and after calibration.

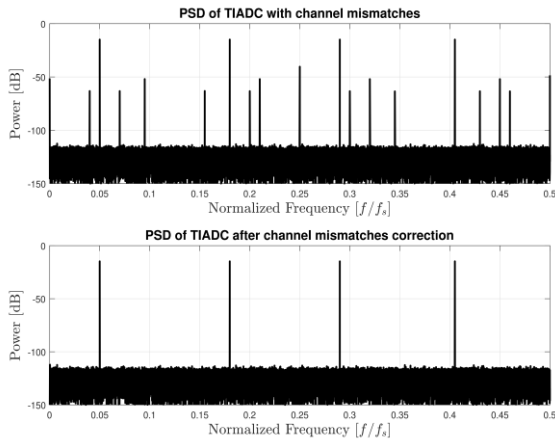


Figure 7. Output spectrum of four-channel TIADC before and after calibration for multi-tone sinusoidal input signal $f_{in} = [0.05 \ 0.18 \ 0.29 \ 0.405] \times f_s$.

the results with published works in [8, 11, 12, 21], the proposed method shows the significant improvements.

In addition, we also simulate proposed techniques for multi-tone sinusoidal input signal which is created at

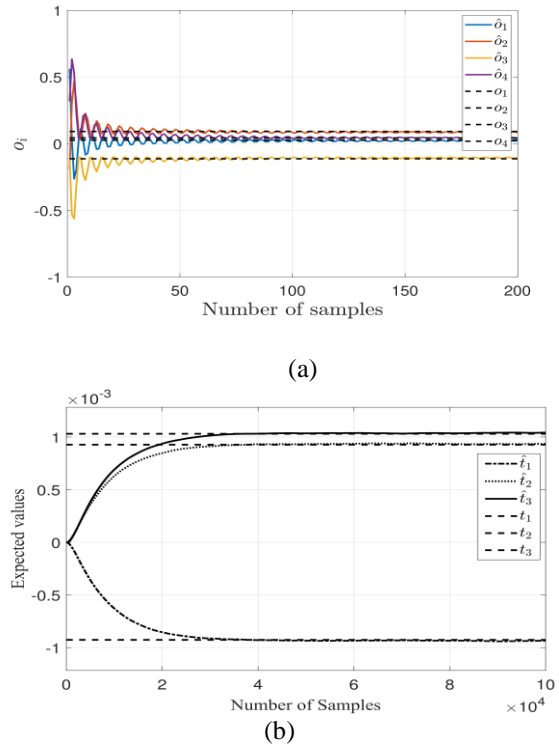


Figure 8. The convergence behavior of channel mismatches: (a) offset mismatch, (b) timing mismatch.

$f_{in} = [0.05 \ 0.18 \ 0.29 \ 0.405] \times f_s$ in the first Nyquist band. The output spectrum of TIADC before and after channel mismatches calibration is shown in Fig. 7. As can be seen, the spurs due to channel mismatches encompassing offset, gain and timing skew are completely removed.

Fig. 8(a) and Fig. (b) shows the convergences of correlation output \hat{o}_i and \hat{t}_i for offset mismatches and timing mismatches. As can be seen, after 25 samples, the offset coefficients \hat{o}_i has converged as in Fig. 8(a). The convergence behavior of the estimated timing coefficients is also very fast. After about 0.3×10^5 samples, the timing coefficients \hat{t}_i has converged.

4.2. Hardware Implementation and Validation

To confirm the effectiveness of the proposed technique, the hardware validation on the FPGA platform was carried out. The FPGA implementation was to validate that the proposed calibration method could be implemented in hardware. The FPGA design and verification flow using hardware co-simulation with MATLAB/Simulink and Xilinx FPGA design tools were utilized in this framework so that a VHDL (Very High Speed Integrated Circuit Hardware Description Language) model of the TIADC was generated from the MATLAB/Simulink model. The hardware architecture of the proposed calibration technique was designed and optimized in terms of fixed point representation characterized by the signal ranges and signal word length optimized by the design tools.

The hardware based verification flow for the proposed technique with the System Generator tool in MATLAB simulation and the Xilinx FPGA-in-the-loop (FIL) methodology is shown in Fig. 9. With the TIADC output generated by the computer, both the conventional simulation by MATLAB and the hardware co-simulation with the FPGA board using the FIL methodology were performed. The TIADC output signal includes all

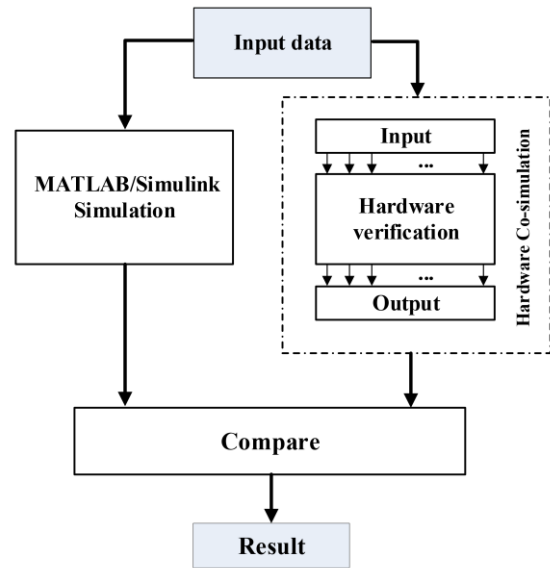


Figure 9. The verification flow for the proposed technique with the system generator tool using MATLAB simulation and FPGA-in-the-loop (FIL).

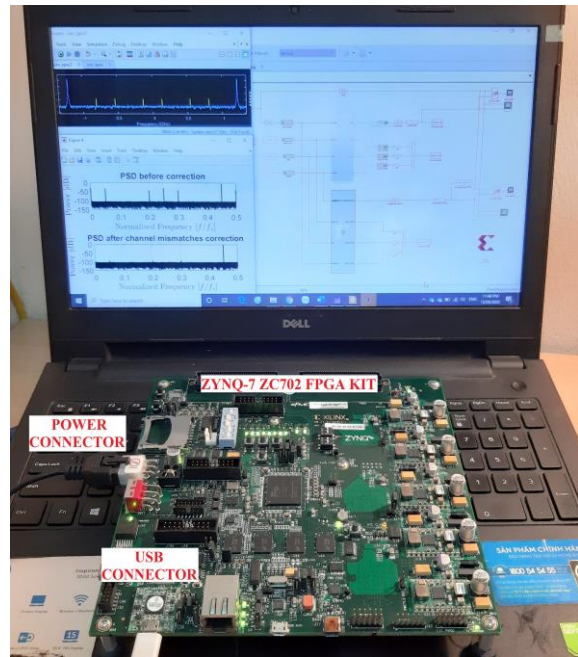


Figure 10. The laboratory measurements for the FPGA based implementation.

deviations as described in Section 2 generated by MATLAB 2019a software on the computer. These signals are then loaded into the FPGA

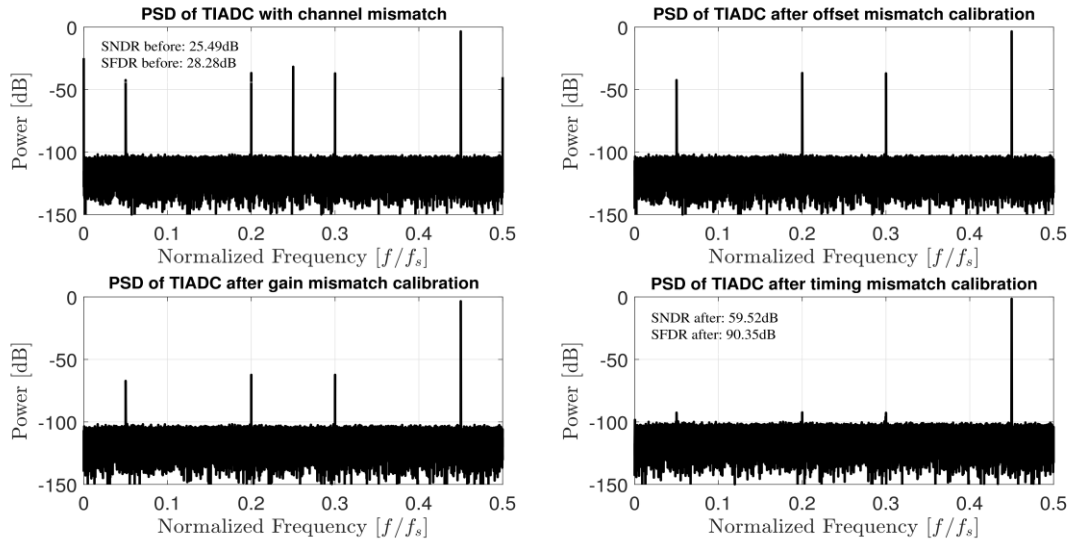


Figure 11. Output spectrum of four-channel TIADC with the proposed technique on FPGA hardware before and after calibration.

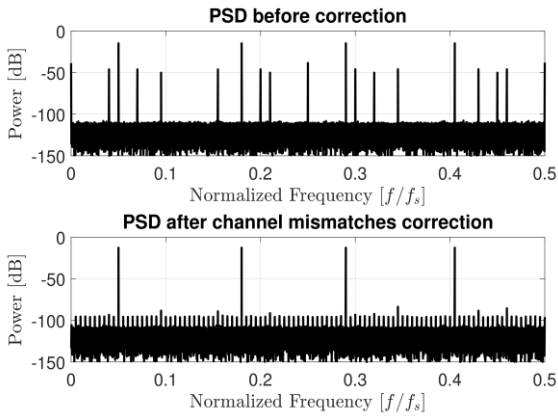


Figure 12. Output spectrum of four-channel TIADC with the proposed technique on FPGA hardware before and after calibration for multi-tone sinusoidal input signal $f_{in} = [0.05 \ 0.18 \ 0.29 \ 0.405] \times f_s$.

Table 2. FPGA implementation results

Device	XC7Z020 CLG484-1 SoC
LUT	9921/53,200 (18.65%)
LUT RAM	61/17,400 (0.35%)
Flip-Flop	7035/106,400 (6.61%)
DSP slices	15/220 (6.82%)

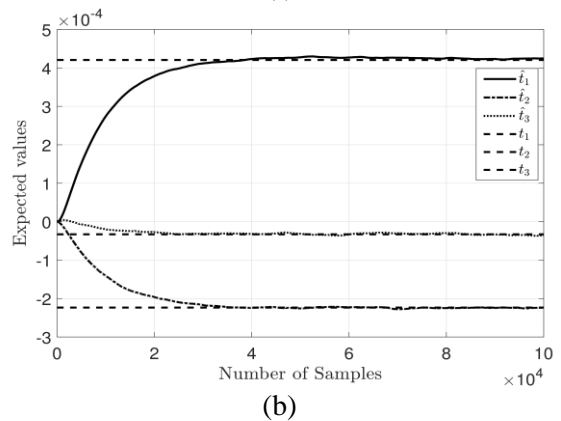
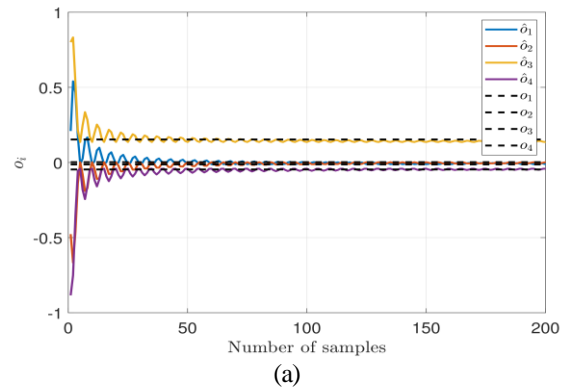


Figure 13. The convergence behavior of channel mismatches: (a) offset mismatch, (b) timing mismatch.

Table 3. The comparison with the state-of-the-art techniques

Characteristics	[12] TCAS-I 2013	[8] TCAS-II 2016	[11] TCAS-I 2018	This work
Mismatch types	Gain, timing	Timing	Offset, gain, timing	Offset, gain, timing
Blind	Yes	Yes	Yes	Yes
Background	Yes	Yes	Yes	Yes
Number of sub-ADC channels	Depend on Hadamard matrix (e.g., 2,4,8...)	4	Any	Depend on Hadamard matrix (e.g., 2,4,8...)
Sampling frequency	--	2.7GHz	32GHz	2.7GHz
Input frequency	$0.45f_s$	Multi-tone	$0.18f_s$	$0.45f_s$ & Multi-tone
Number of bits	10	11	9	11
SNDR improvement (dB)	62	11	36.55	48.1
SFDR improvement (dB)	--	28	43.72	77.98
Convergence time (Samples)	60k	10k	400k	30k

board that has embedded the proposed calibration technique through the JTAG USB cable. The results after hardware execution were fed back into the computer for comparison with the simulation results in MATLAB/Simulink. The results included SNDR, SFDR, the output spectrum, and the convergence time. Fig. 10 illustrates the settings and experimental results of the proposed technique in our laboratory.

Experimental results on the FPGA hardware of the proposed method are shown in Fig. 11, Fig. 12 and Fig. 13. The simulation results in Fig. 6 and Fig. 7 are quite similar the experimental results in Fig. 11 and Fig. 12, respectively. The performance of TIADC before and after calibration on FPGA hardware is also achieved close to simulation. The experimental results show that the performance of the ADC is improved by 34.03 dB for SNDR and 62.07 dB for SFDR. Due to the difference between fixed point and floating point representations, there was still a slight bias in the experimental results.

The convergence behavior of the estimated offset and timing mismatch coefficients on FPGA hardware is shown in Fig. 13(a) and Fig. 13(b), respectively. As can be seen, the

estimated offset \hat{o}_i converges very fast, only after 50 samples. The estimated timing coefficients \hat{t}_i have converged after about 30000 samples. These results are very identical to the simulation ones.

The implementation results on the FPGA hardware (Xilinx ZYNQ-7000 SoC ZC702 evaluation board) demonstrate that the synthesized circuit operates properly and consumes very little hardware resources of the FPGA chip. These results are shown in Table 2.

The comparison results of the proposed technique with the prior state-of-the-arts is shown in Table 3. These results were performed through Monte Carlo simulation. These results were also compared with the simulation results of other techniques. The hardware implementation results of the proposed calibration technique on the FPGA platform were also higher than other techniques. The proposed technique calibrated the offset and gain mismatches with simple calibration techniques before correct the timing mismatch so it reduced the impact on timing mismatch calibration. Therefore the performance of the proposed technique (SNDR and SFDR) is higher than the other techniques. In addition, the adaptation step was selected appropriately so the convergence time is faster.

5. Conclusion

In this paper, a fully digital background calibration technique for offset, gain, and timing mismatches in M -channel TIADC has been presented. The offset mismatch is calibrated by taking the average of output samples of each channel. The gain mismatch is compensated by calculating the power ratio of the sub-ADC with the reference ADC. Finally, timing skew is compensated by combining the LMS adaptive algorithm and the Hadamard matrix. The simulation and implementation results of a 4-channel TIADC has demonstrated a significant improvement in both SNDR and SFDR. In future work, we will consider bandwidth mismatch to further improve the TIADC performance.

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