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Combined Power Ratio Calculation, Hadamard Transform and Least Mean Squares Algorithm for Channel Mismatch Calibration in Time-Interleaved ADCs

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Abstract

This paper presents a method for all-digital background calibration of multiple channel mismatches including offset, gain and timing mismatches in time-interleaved analog-to-digital converters (TIADCs). The average technique is used to remove offset mismatch at each channel. The gain mismatch is calibrated by calculating the power ratio of the sub-ADC over the reference ADC. The timing skew mismatch is calibrated by using Hadamard transform for error correction and the least mean squares (LMS) algorithm for estimation of the clock skew. The performance improvement of TIADCs employing these techniques is demonstrated through numerical simulations.

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1. Introduction

Currently, time-interleaved analog-todigital converters (TIADCs) are known and widely used in high-speed wireless applications [1]. It increases the sampling rate by using multiple channel analog-to-digital converter (ADC) that samples an analog input signal in a time-interleaving manner [2–4]. However, the performance of TIADCs is severely degraded by mismatches between sub-ADCs, including offset, gain, timing, and bandwidth mismatches [4, 5]. Therefore, correcting these mismatches is a very essential requirement.

There have been several works on compensating mismatches in TIADCs [6-17]. Among these works, some researchers calibrate in either all-analog domain [6] or mixed-signal domain [7]. All-analog calibration techniques can be performed with any input signal, but analog estimation is difficult to implement and is not suitable for CMOS technology. Mixed-signal calibration techniques require low power consumption and small chip area. However, its correction is inaccurate and requires an additional analog circuit. Therefore, it reduces the resolution of TIADC and increases the calibration time. Moreover, they are not portable between

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CMOS technology nodes. Thanks to the sinking of CMOS technology, the all-digital calibration is currently preferred, which tackling the gain and timing mismatches, but not dealing with the offset one [8, 9, 12-17]. Thus, in this paper, we propose a method of all-digital background calibration for three deviations including offset, gain and timing mismatches to further enhance the calibration efficiency in TIADC channels. The proposed technique first calibrates the offset error by taking the average of sub-ADC output samples, and then calibrate gain by calculating the power ratio of the sub-ADC with the reference ADC. Finally, timing skew is calibrated by using Hadamard transform for correction and LMS algorithm for estimation.

The proposed technique achieves higher performance and a faster convergence speed compared with the previous techniques. The proposed technique significantly reduces the required hardware resources, specifically for the derivative and fractional delay filters for which no look-up table is required. In addition, the proposed technique requires only one FIR filters with fixed coefficients, thus reducing complexity and hardware resources, as compared to the bank adaptive filter techniques.

The rest of this paper is organized as follows. Section 2 introduces the TIADC model with offset, gain, and timing mismatch. In section 3 we present the proposed technique of all-digital background calibration for channel mismatches. The simulation



Figure 1. Model of a M-channel TIADC with offset, gain and timing mismatches.

results are given in Section 4. Finally, conclusion is carried out in Section 5.

2. System model

Consider the *M*-channel TIADC model consisting of offset, gain, and timing mismatches in Fig. 1. It is characterized by the offset errors o_i , the gain errors g_i and the relative timing deviations t_i for i = 0, 1, ..., M - 1. Without considering the quantization effects, the i^{th} channel's digital output can be expressed as:

$$y_i[k] = g_i x((kM+i)T - t_i) + o_i.$$
 (1)

By assuming a bandlimited input signal $X(j\Omega) = 0$, with $|\Omega| \ge B$ and $B \le \frac{\pi}{T_s}$, the output of *M*-channel TIADC including the errors: offset, gain, timing mismatches errors is expressed as [5]:

$$Y\left(e^{j\omega}\right) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} g_i e^{-j\left(\omega-k\frac{\omega_s}{M}\right)t_i} \cdot e^{jki\frac{2\pi}{M}}\right]$$
$$\times \left(j\left(\omega-k\frac{\omega_s}{M}\right)\right) \tag{2}$$
$$+ \frac{1}{T} \sum_{k=-\infty}^{+\infty} \frac{1}{M} \sum_{i=0}^{M-1} o_i e^{jki\frac{2\pi}{M}} \delta\left(\omega-k\frac{\omega_s}{M}\right).$$

This expression shows that, in the presence of all the errors, the input signal is modulated by the expression between brackets which combines gain and timing mismatch errors. These errors appear at each $\omega_{in} \pm k \frac{\omega_s}{M}$ frequency, where ω_{in} is the input frequency. Additionally, the offset mismatch tones intervene as signal independent spurious tones at each $k \frac{\omega_s}{M}$.

3. Proposed method

The proposed technique performs offset mismatch correction before gain and timing mismatches correction.



Figure 2. Offset mismatch calibration for each sub-ADC.

3.1. Offset calibration

The offset calibration scheme is illustrated in Fig. 2. Assume that \hat{o}_i is the estimate of the offset o_i of the i^{th} channel ADC. Assume that the input signal is Wide-Sense-Stationary (WSS), expected value of the input is approximately zero, i.e. $\frac{1}{N} \sum_{k=0}^{N-1} g_i x((kM + i)T_s - t_i) \approx 0$. Thus, estimated offset values are expressed as follows:

$$\hat{o}_{i} = \frac{1}{N} \sum_{k=0}^{N-1} y_{i}[k]$$

$$= \frac{1}{N} \sum_{k=0}^{N-1} (g_{i}x((kM+i)T_{s} - t_{i}) + o_{i}) \quad (3)$$

$$= \underbrace{\frac{1}{N} \sum_{k=0}^{N-1} g_{i}x((kM+i)T_{s} - t_{i})}_{\approx 0} + o_{i} \approx o_{i}.$$

The offset error can be calibrated by firstly averaging the output of each sub-ADC over N samples as in (3) and then subtracting the average value from the ADC output as follow:

$$\hat{y}_{\text{offset}}[k] = g_i x((kM+i)T - t_i) + o_i - \hat{o}_i$$
$$= g_i x((kM+i)T - t_i). \tag{4}$$

3.2. Gain calibration

The signal after calibration of offset mismatch is expressed in (4). Assuming that g_i denotes the gain mismatch of i^{th} sub-ADC. The goal of gain mismatch estimation is to determine the relative gain of each sub-ADC with respect to a reference ADC, i.e. $\frac{g_i}{g_0}$. Let us assume that the first channel is the reference channel. The authors in [18] obtained the relative gain each sub-ADC by calculating the ratio between the sum of samples' absolute values of ADC to be corrected and the reference ADC. Although this technique is easy for implementation, the performance is not high, especially the spurious-free dynamic range (SFDR). Assuming the power of the channels is the same. Inspired by the calibration method in [18], in this paper, we propose another method to calculate the relative gain. It is obtained by calculating the average power of the i^{th} ADC and the average power of a reference sub-ADC as

$$\frac{\frac{1}{N}\sum_{k=0}^{N-1}y_0^2\left[k\right]}{\frac{1}{N}\sum_{k=0}^{N-1}y_i^2\left[k\right]} = \frac{g_0^2 P_{x(t)}}{g_i^2 P_{x(t)}} = \frac{g_0^2}{g_i^2}.$$
 (5)

This ratio is then taken the square root and multiplied by the i^{th} sub-ADC output to produce the corrected sub-ADC output. This output have the same gain mismatch of the reference sub-ADC as shown in Fig. 3. Therefore, the gain mismatch among sub-ADC channels is the same. Since gain calibration requires adders and multipliers running at the sampling rate of sub-ADCs, it is efficient for the hardware implementation in terms of power consumption and area.

3.3. Timing calibration

3.3.1. Timing mismatch correction

After calibration of offset and gain mismatch, the ADC output is only timing mismatch. Thus, the ADC output can be



Figure 3. Gain mismatch calibration for each sub-ADC.

expressed as

$$y_i[k] = x((kM+i)T - t_i).$$
 (6)

The timing mismatch correction technique is illustrated in Fig. 4. Assume that the sum of the timing mismatch in each channel is equal to zero $t_0 + t_1 + \ldots + t_{M-1} = 0$. The overall output spectrum of the TIADC including only timing mismatch is expressed as [5]:

$$Y\left(e^{j\omega}\right) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \left[\frac{1}{M} \sum_{i=0}^{M-1} e^{-j\left(\omega-k\frac{\omega_s}{M}\right)t_i} \cdot e^{jki\frac{2\pi}{M}}\right] \times X\left(j\left(\omega-k\frac{\omega_s}{M}\right)\right).$$
(7)

Without loss of generality, we consider the *M*-channel model without a quantization noise. $F_k(j\omega)$, k = 0, 1, ..., M-1 are channel responses, where $-\pi < \omega \leq \pi$. Since $F_k(j\omega)$ have only timing mismatch, these channel responses are expressed as

$$F_k(j\omega) = e^{j\omega(k-t_i)}.$$
 (8)

To calibrate timing mismatch, we use Hadamard transform multiplied by the output signal of the ADC. This signal is called an error signal which is used to removing timing skew.

$$\mathbf{y}_t'[n] = y[n]\mathbf{H}[n] * h_d[n], \qquad (9)$$

where $\mathbf{H}[n]$ is the Hadamard matrix of order $M, h_d[n]$ is the impulse response of the derivative filter.

$$h_d[n] = \begin{cases} \frac{\cos(n\pi)}{n} & (n \neq 0) \\ 0 & (n = 0) \end{cases} .$$
(10)

The calibrated signal is calculated by subtracting the error signal from the TIADC output [19].

$$\hat{y}[n] = y[n] - \omega_{ti} \mathbf{y}'_t[n]. \tag{11}$$

The filter coefficients are determined by multiplying the exact coefficients with the Hanning window function. The coefficients ω_{ti} are calculated based on the sign of the Hadamard matrix as follows:

$$\begin{bmatrix} \omega_{t0} \\ \omega_{t1} \\ \vdots \\ \omega_{t(M-1)} \end{bmatrix} \approx \frac{1}{M} \mathbf{H} \begin{bmatrix} t_0 \\ t_1 \\ \vdots \\ t_{M-1} \end{bmatrix}.$$
(12)

where t_i i = 0, 1, ..., M - 1 is much less than 1 and $\omega_{t0} = 0$.

3.3.2. Timing mismatch estimation

In this section, we present the structure of the timing mismatch estimation block as shown in Fig. 5. The timing mismatch estimation block gives timing mismatch coefficients $\hat{\omega}_{ti}$ by using the LMS algorithm. These estimated values are used to create the estimated error signal $\hat{y}'_t[n]$. This signal is then subtracted from y[n] to obtain the restored signal $\hat{y}[n]$ as

$$\hat{y}[n] = y[n] - \hat{y}'_t[n],$$
 (13)

where

$$\hat{y}_t'[n] = \hat{\omega}_{\mathbf{t}\mathbf{i}} \bar{\mathbf{y}}_t'[\mathbf{n}], \qquad (14)$$

with $\bar{\mathbf{y}}'_{\mathbf{t}}[\mathbf{n}]$ are generated by the FIR filter f[n] and Hadamard transform H[n] as in (15). This technique requires only one FIR filter for M-channel estimation. Thus, the circuit area is reduced.

$$\bar{\mathbf{y}}_{\mathbf{t}}'[\mathbf{n}] = y[n]\mathbf{H}[\mathbf{n}] * h_d[n] * f[n].$$
(15)

Timing mismatch coefficients $\hat{\omega}_{ti}$ can be calculated from an updating of the correlation



Figure 4. The calibration diagram for the timing mismatch in TIADC.



Figure 5. The timing mismatch estimation block.

Table 1. The table of channel mismatch values

Sub	Channel mismatches					
ADC	O_i	g_i	t_i			
ADC_0	0.026883	0.0365	0			
ADC_1	0.091694	-0.00481	$-0.00092685T_s$			
ADC_2	-0.01129	-0.0047	$0.00092685T_s$			
ADC_3	0.043109	0.00782	$0.0010306T_s$			

by the LMS algorithm

$$\hat{\omega}_{\mathbf{t}}[\mathbf{n}] = \hat{\omega}_{\mathbf{t}}[\mathbf{n} - \mathbf{1}] + \mu \bar{\mathbf{y}}'_{\mathbf{t}}[\mathbf{n}] \varepsilon[n], \qquad (16)$$

where μ is the step-size parameter for LMS algorithm, whereas $\varepsilon[n]$ are delayed versions of y[n] after the high-pass filter f[n].

4. Simulation results

To illustrate the proposed techniques, we simulate the calibration method by using the Matlab software. A 33-tap correction FIR filter, 11-bit ADC quantization, and a sampling frequency of 2.7GHz are used. The correction FIR filter is designed with the Hanning window for truncation and delay. To show the effectiveness of the proposed method, the simulated results of a four-channel TIADC are shown, assuming that the channel 0 without timing mismatch is the reference channel for timing mismatch calibration, as demonstrated in Table 1. The input signal is bandlimited with a variance $\sigma = 1$ and 2^{18} sample, LMS algorithm with adaptive step $\mu = 2^{-15}$. The signal-to-noise ratio (SNR) is calculated according to equation 17, 18 for

$$y[n] \text{ and } \hat{y}[n] \text{ as } [13]$$

 $SNR_y = 10 \log_{10} \left(\frac{\sum_{n=0}^{N-1} |x[n]|^2}{\sum_{n=0}^{N-1} |x[n] - y[n]|^2} \right),$
(17)

$$SNR_{\hat{y}} = 10 \log_{10} \left(\frac{\sum_{n=0}^{N-1} |x[n]|^2}{\sum_{n=0}^{N-1} |x[n] - \hat{y}[n]|^2} \right).$$
(18)

The simulation results in Fig. 6 show the output spectrum before and after channel calibration for mismatches single-tone sinusoidal input signal which is created at $f_{in} = 0.45 \times f_s$. The proposed technique has completely eliminated all channel mismatches. The signal-to-noise-and-distortion ratio (SNDR) after calibration is 67.2 dB which leads to an improvement of 48.10 dB compared with the uncompensated output. Moreover, SFDR after calibration is 97.89 dB equivalent to an improvement of 77.98 dB compared with the uncompensated Thus, the performance of TIADC output. is significantly improved. Comparing the results with published works in [8, 11, 12, 20], the proposed method shows the significant improvements.

In addition, we also simulate proposed techniques for multi-tone sinusoidal input signal which is created at $f_{in} = [0.05 \ 0.18 \ 0.29 \ 0.405] \times f_s$ in the first Nyquist band. The output spectrum of



Figure 6. Output spectrum of four-channel TIADC before and after calibration.



Figure 7. Output spectrum of four-channel TIADC before and after calibration for multi-tone sinusoidal input signal $f_{in} = [0.05 \ 0.18 \ 0.29 \ 0.405] \times f_s.$



(a) The convergence of the offset mismatch coefficients $\hat{o}_i.$



(b) The convergence of the timing mismatch coefficients $\hat{\omega}_{ti}$.

Figure 8. The convergence behavior of channel mismatches: (a) offset, (b) timing mismatch

TIADC before and after channel mismatches calibration is shown in Fig. 7. As can be seen, the spurs due to channel mismatches encompassing offset, gain and timing skew are completely removed.

Fig. 8(a) and Fig. 8(b) shows the convergences of correlation output o_i and ω_{ti} for offset mismatches and timing mismatches. As can be seen, after 25 samples, the offset coefficients \hat{o}_i has converged as in Fig. 8(a). The convergence behavior of the estimated timing coefficients is also very fast. After about 0.3×10^5 samples, the timing coefficients $\hat{\omega}_{ti}$ has converged.

The comparison results of the proposed technique with the prior state-of-the-arts is shown in Table 2. The simulation results in this table have clarified the improvement of the proposed technique in both the system performance and the convergence time.

5. Conclusion

In this paper, an all-digital background calibration technique for offset, gain, and timing mismatches in M-channel TIADC has been presented. The offset mismatch is calibrated by taking the average of output samples of each channel. The gain mismatch is compensated by calculating the power ratio of the sub-ADC with the reference ADC. Finally, timing skew is compensated by combining the LMS adaptive algorithm and the Hadamard matrix. The simulation results of a 4-channel TIADC has demonstrated a significant improvement in both SNDR and SFDR. In future work, we will consider bandwidth mismatch to further improve the TIADC performance.

References

- I. Melamed, S. Toledo, A robust, selective, and flexible rf front-end for wideband sampling receivers, ICT Express 3 (2) (2017) 96–100.
- [2] W. C. Black, D. A. Hodges, Time interleaved converter arrays, IEEE Journal of Solid-state circuits 15 (6) (1980) 1022–1029.
- B. Razavi, Design considerations for interleaved adcs, IEEE Journal of Solid-State Circuits 48 (8) (2013) 1806–1817.
- [4] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, K. Kobayashi, Explicit analysis of channel mismatch effects in time-interleaved adc

	[10]	[0]	[11]	TTL:
	[12]	[8]	[11]	This
Characteristics	TCAS-I 2013	TCAS-II 2016	TCAS-I 2018	work
Mismatch types	Gain, timing	Timing	Offset, gain, timing	Offset, gain, timing
Blind	Yes	Yes	Yes	Yes
Background	Yes	Yes	Yes	Yes
Number of sub-ADC channels	Any	4	Any	Any
Sampling frequency	_	$2.7 \mathrm{GHz}$	$32 \mathrm{GHz}$	$2.7 \mathrm{GHz}$
Input frequency	$0.45 f_{s}$	Multi-tone	$0.18 f_{s}$	$0.45 f_s$ & Multi-tone
Number of bits	10	11	9	11
SNDR improvement (dB)	62	11	36.55	48.1
SFDR improvement (dB)	_	28	43.72	77.98
Convergence time (Samples)	60k	10k	400k	30k

Table 2. The comparison with the state-of-the-art techniques

systems, IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications 48 (3) (2001) 261–271.

- [5] C. Vogel, The impact of combined channel mismatch effects in time-interleaved adcs, IEEE transactions on instrumentation and measurement 54 (1) (2005) 415–427.
- [6] P. J. Harpe, J. A. Hegt, A. H. van Roermund, Analog calibration of channel mismatches in time-interleaved adcs, International Journal of Circuit Theory and Applications 37 (2) (2009) 301–318.
- [7] D. Camarero, K. B. Kalaia, J.-F. Naviner, P. Loumeau, Mixed-signal clock-skew calibration technique for time-interleaved adcs, IEEE Transactions on Circuits and Systems I: Regular Papers 55 (11) (2008) 3676–3687. doi:10.1109/TCSI.2008.926314.
- [8] H. Le Duc, D. M. Nguyen, C. Jabbour, T. Graba, P. Desgreys, O. Jamin, et al., All-digital calibration of timing skews for tiadcs using the polyphase decomposition, IEEE Transactions on Circuits and Systems II: Express Briefs 63 (1) (2016) 99–103.
- [9] H. Le Duc, D. M. Nguyen, C. Jabbour, T. Graba, P. Desgreys, O. Jamin, et al., Hardware implementation of all digital calibration for undersampling tiades, in: Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, IEEE, 2015, pp. 2181–2184.
- [10] L. Guo, S. Tian, Z. Wang, Estimation and correction of gain mismatch and timing error in time-interleaved adcs based on dft, Metrology and Measurement Systems 21 (3) (2014) 535–544.
- [11] Y. Qiu, Y.-J. Liu, J. Zhou, G. Zhang, D. Chen, N. Du, All-digital blind background calibration technique for any channel time-interleaved adc, IEEE Transactions on Circuits and Systems I: Regular Papers 65 (8) (2018) 2503–2514.
- [12] J. Matsuno, T. Yamaji, M. Furuta, T. Itakura, All-digital background calibration technique for time-interleaved adc using pseudo aliasing signal, IEEE Transactions on Circuits and Systems I: Regular Papers 60 (5) (2013) 1113–1121.
- [13] S. Saleem, C. Vogel, On blind identification of gain and timing mismatches in time-interleaved analog-to-digital converters, in: 33rd International

Conference on Telecommunications and Signal Processing, Baden (Austria), Citeseer, 2010, pp. 151–155.

- [14] H.-W. Kang, H.-K. Hong, S. Park, K.-J. Kim, K.-H. Ahn, S.-T. Ryu, A sign-equality-based background timing-mismatch calibration algorithm for time-interleaved adcs, IEEE Transactions on Circuits and Systems II: Express Briefs 63 (6) (2016) 518–522.
- [15] H.-H. Chen, J. Lee, J.-T. Chen, Digital background calibration for timing mismatch in time-interleaved adcs, Electronics Letters 42 (2) (2006) 74–75.
- [16] S. Liu, N. Lv, H. Ma, A. Zhu, Adaptive semiblind background calibration of timing mismatches in a two-channel time-interleaved analog-to-digital converter, Analog Integrated Circuits and Signal Processing 90 (1) (2017) 1–7.
- [17] H. Chen, Y. Pan, Y. Yin, F. Lin, All-digital background calibration technique for timing mismatch of time-interleaved adcs, Integration, the VLSI Journal 57 (2017) 45–51.
- [18] N. Le Dortz, J.-P. Blanc, T. Simon, S. Verhaeren, E. Rouat, P. Urard, S. Le Tual, D. Goguet, C. Lelandais-Perrault, P. Benabes, 22.5 a 1.62 gs/s time-interleaved sar adc with digital background mismatch calibration achieving interleaving spurs below 70dbfs, in: 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), IEEE, 2014, pp. 386–388.
- [19] S. Tertinek, C. Vogel, Reconstruction of nonuniformly sampled bandlimited signals using a differentiator-multiplier cascade, IEEE Transactions on Circuits and Systems I: Regular Papers 55 (8) (2008) 2273–2286.
- [20] C. Cho, J.-G. Lee, P. D. Hale, J. A. Jargon, P. Jeavons, J. Schlager, A. Dienstfrey, Calibration of channel mismatch in time-interleaved real-time digital oscilloscopes, in: Microwave Measurement Conference (ARFTG), 2015 85th, IEEE, 2015, pp. 1–5.